Advanced Mathematics
MEVD 101

Unit 1 : Partial Differential Equation
Solution of Partial Differential Equation (PDE) by separation of variable method, Numerical solution of PDE (Laplace, Poisson's, Parabola) using finite difference Methods.

Unit 2 : Matrices And Linear System Of Equations
Solution of linear simultaneous equations by Gaussian elimination and its modification, Crout's triangularization method, Iterative methods-Jacobins method, Gauss-Seidal method, Determination of Eigen values by iteration.

Unit 5 : Calculus Of Variations
Euler-Lagrange's differential equation, The Brachistochrone problems and other applications. Isoperi-metric problem, Hamilton's Principle and Lagrange's Equation, Rayleigh-Ritz method, Galerkin method.

Unit 4 : Fuzzy Logic
Operations of fuzzy sets, fuzzy arithmetic & relations, fuzzy relation equations, fuzzy logics. MATLAB introduction, programming in MATLAB scripts, functions and their
application.

Unit 5 : Reliability
Introduction and definition of reliability, derivation of reliability functions, Failure rate, Hazard rate, mean time t future & their relations, concepts of fault tolerant analysis.

Reference Books:
1. Higher Engineering Mathematics - by Dr. B.S. Grewal; Khanna Publishers
2. Calculus of Variations - by Elsgole; Addison Wesley.
3. Applied Numerical Methods with MATLAB by Steven C Chapra, TMH.
4. Introductory Methods of Numerical Analysis by S.S. Shastry,
5. Calculus of Variations - by Galfand & Fomin; Prentice Hall.
6. Higher Engineering Mathematics by B.V. Ramana, Tata Mc Hill.
7. Advance Engineering Mathematics by Ervin Kreszig, Wiley Easten Edd.
8. Numerical Solution of Differential Equation by M. K. Jain
9. Numerical Mathematical Analysis By James B. Scarborogh
10. Fuzzy Logic in Engineering by T. J. Ross
11. Fuzzy Sets Theory & its Applications by H. J. Zimmersoms

VLSI Design Concepts

MEVD-102

UNIT – I : Introduction to CMOS circuits:
MOS transistors, MOS switches, CMOS logic: Inverter, combinational logic, NAND, NOR gates, compound gates, Multiplexers. Memory: Latches and registers. Circuit and system representations: Behavioral, structural and physical representations.

UNIT – II : MOS transistor theory:
NMOS, PMOS enhancement mode transistors, Threshold voltage, body effect, MOS device design equations, MOS models, small signal AC characteristics, CMOS inverter DC characteristics, static load MOS inverters, Bipolar devices - advanced MOS modeling – large signal and small signal modeling for BJT.

UNIT – III : LOW – VOLTAGE LOW POWER VLSI CMOS CIRCUIT DESIGN:
CMOS invertor – Characteristics – Power dissipation. Capacitance estimation. CMOS static logic design, Logic styles.

UNIT – IV
Circuit characterization and performance estimation: Estimation of resistance, capacitance, inductance. Switching characteristics, CMOS gate transistor sizing, power dissipation, sizing routing conductors, charge sharing, Design margining yield, reliability. Scaling of MOS transistor dimensions.

UNIT – V
CMOS circuit and logic design: CMOS logic gate design, physical design of simple logic gates. CMOS logic structures. Clocking strategies, I/O Structures.

References

1. Weste, Eshraghian, "Principles of CMOS VLSI design", 2nd Edition Addison Wesley, 1994.
2. Douglas A Pucknell and Kamaran Eshragian, " Basic VLSI design ", 3rd edition, PHI, 1994.
3. BELLAOUR & M.I.ELAMSTRY, "Low – Power Digital VLSI Design, Circuits and Systems", Kluwer Academic Publishers, 1996.
4. S.IMAM & M.PEDRAM, "Logic synthesis for Low – Power VLSI Designs", Kluwer Academic publishers, 1998.
5. B.G.K.YEAP, "Practical Low Power Digital VLSI Design", Kluwer Academic publishers, 1998.

Modeling of Digital Systems using HDL

MEVD-103

UNIT – I Introduction to PLDs & FPGAs
ROMs, Logic array (PLA), Programmable array logic, GAL, bipolar PLA, NMOS PLA, PAL 14L4, Xilinx logic cell array (LCA) – I/O Block – Programmable interconnect – Xilinx – 3000 series and 4000 series FPGAs. Altera CPLDs, altera FLEX 10K series PLDs.

UNIT – II Placement and routing
Mincut based placement – iterative improvement placement– Routing: Segmented channel routing – Maze routing – Routability and routing resources – Net delays.

UNIT – III Introduction to VHDL
Digital system design process – Hardware simulation – Levels of abstraction – VHDL requirements – Elements of VHDL – Top down design VHDL operators – Timing – Concurrency – Objects and classes – Signal assignments – Concurrent and sequential assignments.

UNIT – IV Structural, Data flow & Behavioral description of hardware in VHDL
Parts library – Wiring of primitives – Wiring of iterative networks – Modeling a test bench – Top down wiring components – Subprograms. Multiplexing and data selection – State machine descriptions – Open collector gates – Three state bussing. - Process statement – Assertion statement – Sequential wait statements – Formatted ASCII I/O operations MSI based design.

UNIT – V Introduction to Verilog HDL
Lexical conventions – Data types – System tasks and Compiler Directives- Modules and Ports- Gate Level Modeling with Examples.

References
P.K. Chan & S. Mourad, "Digital Design sing Field Programmable Gate Array" 1st Edition, Prentice Hall, 1994.
J. V. Old Field & R.C. Dorf, " Field Programmable Gate Array", John Wiley, 1995.
M. Bolton, " Digital System Design with Programmable Logic", Addison Wesley, 1990.
Thomas E. Dillinger, " VLSI Engineering", Prentice Hall, 1st Edition, 1998.
Douglas Perry, "VHDL", 3rd Edition, McGraw Hill 2001.
J. Bhasker, "VHDL", 3rd Edition, Addison Wesley, 1999

Advanced Digital Signal Processing
MEVD-104

Unit 1 : Discrete Time signals - sequences, representation
Discrete Time Systems Linear, Time invariant, LTI System, properties, constant coefficient difference equation. Frequency Domain Representation of discrete time signals & systems

Unit 2 : Discrete Time Random Signals
Z Transform properties, R.O.C, stability, Causality criterion,Inverse Z- Transform , Recursive and Non recursive systems, Realization of discrete time system.

Unit 3 : D.F.T â " properties, linear and circular convolution
Discrete Cosine transform, relationship between DFT & DCT, I.D.F.T , computation of D.F.T : F.F.T â " Decimation in time & Decimation in frequency.

Unit 4 : F.I.R and I.I.R Systems :
Basic structure of FIR & IIR, Bilinear transformation, Design of discrete time I.I.R filters â " Butterworth, Chebychev, Inv. Chebychev, elliptic etc. Design of F.I.R filters by windowing â " rectangular,Bartlett, Hann, Hamming, Kaiser window filter , Design method , Relationship of Kaiser to other windows. Application of MATLAB for design of digital filters Effect of finite register length in filter design.

Unit 5 : Advanced signal processing techniques and transforms:
Multirate Signal processing Down sampling/upsampling, Int. to discrete Hilbert transform, wavelet transform, Haar transform etc. Application of DSP to Speech Signal Processing.

References :
1. A.V Opprenheim and R.W Schaffer, â œDiscrete â " Time signalprocessingâ (2nd edition) , Prentice Hall
2. S. Mittra Digital Signal Processing using MATLAB, 2nd Edition.
3. Proakis, Int. to Digital Signal Processing, Maxwell Mcmillan.

VLSI Technologies
MEVD -105

UNIT –I: Review of Microelectronics and Introduction to MOS Technologies:
MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:
Layout Design and Tools:
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:
Combinational Logic Networks:
Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:
Sequential Systems:
Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V:
Floor Planning:
Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

Reference:
1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
4. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.