		Part A Int	rodu	ction		
Program : Class : BCA I Se		Class : BCA I Semes	ter	Year : 2022	Sess	ion : 2022-23
Certificate						
1	Course Code S1-BCAA1T					
2	Course Title		Computer Fundamentals, Organization &			
2	Course Type (	Coro	Architecture			
5	Course / Electiv	ve/Generic	Major – raper i			
	Elective/Voca	tional)				
4	Pre-Requisite	(if any)	To bas	Study This Cours ic knowledge of con	e, a stu mputers	ident must have
5	Course Learning outcomes (CLO)       After the construction successful studie         • Under operation operat		<ul> <li>er the completion cessful student will</li> <li>Understand operation and computer.</li> <li>Design simplicircuits based</li> <li>Understand the and logic unit.</li> <li>Know about system includ virtual memore</li> <li>Know the correlated technor the field of correlated technor Credits</li> </ul>	<ul> <li>bletion of this course, a</li> <li>will be able to:</li> <li>and the basic structure,</li> <li>and characteristics of digital</li> <li>imple combinational digital</li> <li>ased on given parameters.</li> <li>and the working of arithmetic</li> <li>unit.</li> <li>bout hierarchical memory</li> <li>cluding cache memories and</li> <li>emory.</li> <li>e contributions of Indians in</li> <li>of computer architecture and</li> <li>chnologies.</li> </ul>		
7	Total Marks		Ма	x. Marks : 100	Min. M	1arks : 40
	<b>x</b> 1	Part B - Con	tent	of the Course		
	N	<u>u. ut Lectures (In nours)</u> Total no. of	i per Lect	weekj : 2 Hours po ures: 60 Hrs	er week	<u>i</u>
Unit		Topics	ысы	ui coi ov 1113.		No. of
					Lectures	
	<b>Fundamentals of Computers:</b> Definition, Characteristics, Capabilities				8	
1	and limitations.					
	computers. Work station, server computers, generations of computers					
	Smart systems: definition, characteristics and applications. Definition					
	embedded system, GIS, GPS, Cloud computing.					
	services.					
	Block diagram of computer and its functional units. Concept of					
2	hardware, software and firmware. Types of software.				•	10

	<b>Input devices –</b> keyboard, scanner, mouse, light pen, bar code reader, OMR, OCR, MICR, Trach ball, joystick, touch screen camera, mic etc. <b>Output devices – Monitors –</b> monitors – classification of monitors based on technology – CRT & Flat panel, LCD, LED monitors, speakers, printers- dot matrix printer, ink jet printer, laser printer, 3D printers, Wi-Fi enabled printers, plotters and their types, LCD/LED Projectors. Computer memory and its types, storage devices: magnetic tapes, Floppy Disks, Hard disks, compact disc- CD-ROM, CD-RW, VCD, DVD, DVD-RW, USB drives, Blue ray disc, SD/MMC Memory Cards.	
3	<ul> <li>Fundamentals of digital electronics: Data types, complements, fixed-point representation, floating-point representation, Binary and other codes, Error detection codes.</li> <li>Logic Gates, Boolean Algebra, map simplification, Combinational Circuits, Sequential circuits, simple combinational circuit design problems.</li> <li>Combinational Circuits – Adder – sub tractor, multiplexer, Demultiplexer, Decoders, Encoders.</li> <li>Sequential Circuits – Flip-Flops, Registers, counters.</li> </ul>	10
4	Basic Computer Organization: Instruction codes, computerregisters, computer instructions, timing & control, instruction cycles,memory reference instruction, input-output & interrupts.Instruction formats, addressing modes, instruction codes, machinelanguage, and assembly language.Register Transfer and Micro operations: Register transfer language,register transfer, Bus & memory transfer, arithmetic Micro-operation,logic micro-operations, shift Micro-operations.	10
5	<ul> <li>Processor and control unit: Hardwired vs. micro programmed control unit, general register organization, stack organization, instruction format, data transfer &amp; manipulation, program control, introductory concept of RISC, CISC, advantages and disadvantages of both.</li> <li>Pipelining – Concept of pipelining, introduction to pipelined data path and control – handling data hazards &amp; control hazards.</li> </ul>	10
6	<ul> <li>Memory and I/O systems – Peripheral devices, I/O interface.</li> <li>Data transfer schemes- Program control, Interrupt, DMA transfer, I/O Processor.</li> <li>Memory Hierarchy, Processor Vs. Memory Speed, High-speed memories, main memory &amp; its types, Auxiliary memory, cache memory, associative memory, interleaving, concept of virtual memory, Hardware support for memory management.</li> </ul>	10
7	Indian contribution to the field –Contributions of reputed scientists of Indian origin like – Dr. Vinod Dham – Father on Intel Pentium Processor, Dr. Ajay Bhat – Co-inventor of USB technology, Dr. Vinod Khosla Co-Founder of Sun Microsystems, Dr. Vijay P Bhatkar – Architect of India's national initiative in supercomputing, and many others.	2

Parallel Computing projects of India – PARMA, ANUPAM, FLOSOLVER, CHIPPS etc. other relevant contributors and contributions.

#### **Part C- Learning Resources** Text Books, Reference Books, Other resources

#### **Text Books:**

- M. Morris Mano, "Computer System Architecture", PHI. •
- Heuring Jordan, "Computer system Design & Architecture" (A.W.L.) •
- मध्य प्रदेश हिंदी ग्रंथ अकादमी से प्रकाशित विषय से संबंधित पस्तकें •

#### **Reference Books:**

- William Stalling, "Computer Organization & Architecture", Pearson Education Asia. •
- V. Carl Hamacher, "Computer Organization", TMH •
- Tannenbaum, "Structured Computer Organization", PHI. •
- Er. Rajiv Chopra, Computer Architecture", Revised 3<sup>rd</sup> Edition, S. Chand & company Pvt. Ltd. •

#### Suggested digital platform web links:

https://www.youtube.com/watch?v+=4TzMyXmzL8M https://nptel.ac.in/courses/106/106/106106166 https://nptel.ac.in/courses/106/106/106106134 Suggested equivalent online courses:

https://nptel.ac.in/courses/106/105/106105163

Part D- Assessment and Evaluation				
Internal Assessment:		External assessment: Un	niversity exam (UE):	
<b>Continuous Comprehe</b>	nsive	marks		
Evaluation (CCE) :		Time: 02.00 Hours		
Shall be based on allotte	ed assignments and class			
tests. The marks shall be	e as follows:			
Assessment and				
presentation of				
assignment				
Class Test I				
(Objective				
Questions)				
Class Test I				
(Descriptive				
Questions)				
Total		Total	100 Marks	
Any remarks / suggestions: Theoretical exposition should be accompanied by Discussions, Case-				

studies preferably with Indian Context, Presentations and Industry Based Assignments.

Part A Introduction						
Program :		Class : BCA I SEM		Year : 2022	Sess	ion : 2022-23
Certificate						
1	Course Code			S1-	BCAA1P	
2	Course Title		Cor	nputer Fundament	tals, and	Digital lab
3	Course Type	(Core	Major – Paper I			
	Course/Elect	ive/Generic				
	Elective/Voca	ational)				
4	Pre-Requisite	e (if any)	Open for All			
5	Course Learning outcomes (CLO)		<ul> <li>successful student will be able to:</li> <li>Familiarity with parts of the computer and peripheral devices used with computer.</li> <li>Realization of the basic logic and universal gates.</li> <li>Verify the behavior of logic gates using truth tables.</li> <li>Implement Binary-to-Gray, Gray-to Binary code conversions.</li> <li>Design half and full adder circuit using basic gates.</li> <li>Design and construct flip flops and marife the avaitation to black</li> </ul>			
6	Credit Value Practical – 2 Credits					
7	Total MarksMax. Marks : 100Min. Marks : 40				Aarks : 40	
		Part B - Cont	tent	of the Course		
		No. of Lectures (in hours	per	week) : 1 Hours p	er week	<u> </u>
	1	Total no. of	Lect	ures: 30 Hrs.		
Unit		Topics				No. of
						Lectures
	I. Co a. Idd ex b. Idd SM c. Idd SM c. Idd II. Di a. Ve NC b. Ve	tify various parts of the computer by physical nination. htify various parts inside the CPU like motherboard, PS, ports buses, IC chips, Processor, HDD, and RAM etc. htify various I/O devices available in the lab physically. tal Electronics ification and interpretation of truth table for AND, OR, Gates. ification and interpretation of truth table for NAND, R gates.			30 Hrs.	
	c. Ve	rification and interpretation	on of	truth table for Ex-	OR, Ex-	

	NOR gates.	
d.	Study of half adder using XOR and NAND gates and	
	verification of its operation.	
e.	Study of full adder using XOR and NAND gates and	
	verification of its operation.	
f.	Study of half subtractor and verification of its operation.	
g.	Study of full subtractor and verification of its operation.	
h.	Realization of logic functions with the help of NAND-	
	Universal gates.	
i.	Realization of logic functions with the help of NOR-	
	Universal gates.	
j.	Verify the truth table of RS flip-flops using NAND and NOR	
	gates.	
k.	Verify the truth table of JK flip-flops using NAND and NOR	
	gates.	
l l.	Verify the truth table of T and D flip-flops using NAND and	
	NOR gates.	
m.	Implementation of 4xl multiplexer using logic gates.	
n.	Implementation of 1x4 demultiplexer using logic gates.	
0.	Verify Gray to Binary conversion using NAND gates only.	
p.	Verity Gray to Binary conversion using NAND gates only.	

# Part C- Learning Resources

#### Text Books, Reference Books, Other resources

#### **Text Books:**

- M. Morris Mano, "Computer System Architecture", PHI.
- Heuring Jordan, "Computer system Design & Architecture" (A.W.L.)
- मध्य प्रदेश हिंदी ग्रंथ अकादमी से प्रकाशित विषय से संबंधित पुस्तकें

### **Reference Books:**

- William Stalling, "Computer Organization & Architecture", Pearson Education Asia.
- V. Carl Hamacher, "Computer Organization", TMH
- Tannenbaum, "Structured Computer Organization", PHI.

## Suggested digital platform web links:

https://de-iitr.vlabs.ac.in/

# Suggested equivalent online courses:

https://nptel.ac.in/courses/106/105/106105163

Part D- Assessment and Evaluation					
Internal Assessment:		External assessment: University exam (UE):			
Continuous Comprehen	sive	Time: 02.00 Hours			
Evaluation (CCE) :					
Shall be based on allotted	d assignments and class				
tests. The marks shall be	as follows:				
Hand-on Lab practice					
Viva					
Lab Test from Practical					
Assignments (Chats /					

model) / Technology		
Dissemination /		
Excursion / lab visit /		
industrial training		
Total	Total	100 Marks
Excursion / lab visit /		
Industrial		
Training is compulsory		