Sri Satya Sai University of Technology & Medical Sciences, Sehore (M.P.)

Scheme of Examination

Third Semester –M.Tech. (VLSI Design)

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End Sem. Exam.	Tests (Two)	Assignments /Quiz	End Sem. Practical / Viva	Practical Record/ assignment/ Quiz/Presentation	
1.	MEVD-301	Elective 1	3	1	-	4	70	20	10	-	-	100
2.	MEVD-302	Elective 2	3	1	-	4	70	20	10	-	-	100
3.	MEVD-303	Seminar			4	4				-	100	100
4.	MEVD-304	Dissertation Part I			8	8				120	80	200
		Total	6	2	12	24	140	40	20	120	180	500

Elective 1 (A) CAD for VLSI Circuits (B) Design for Testability

Elective 2 (A) VLSI SIGNAL PROCESSING (B) Low Power and High Speed VLSI Design

L: Lecture- T: Tutorial- P: Practical *w.e.f. July- 2014*