Sri Satya Sai University of Technology & Medical Sciences, Sehore (M.P.)

Scheme of Examination

Second Semester –M.Tech. (VLSI Design)

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End Sem. Exam.	Tests (Two)	Assignments/ Quiz	End Sem. Practical / Viva	Practical Record/ assignment/Quiz/ Presentation	
1.	MEVD-201	Design of Analog/Mixed Mode VLSI Circuits	3	1	-	4	70	20	10	-	-	100
2.	MEVD-202	ASIC Design And FPGAs	3	1	-	4	70	20	10	-	-	100
3.	MEVD-203	Embedded Real Time Operating Systems	3	1	-	4	70	20	10	-	-	100
4.	MEVD-204	Embedded Systems	3	1	-	4	70	20	10	-	-	100
5.	MEVD-205	System on Chip	3	1	-	4	70	20	10	-	-	100
6.	MEVD-206	Lab -1 : Designing with FPGAs	-	-	6	6	-	-	-	90	60	150
7.	MEVD-207	Lab -2 : Digital Signal Processing And Embedded System	-	-	6	6	-	-	-	90	60	150
		Total	15	5	12	32	350	100	50	180	120	800

L: Lecture- T: Tutorial- P: Practical

w.e.f. July- 2014