Sri Satya Sai University of Technology & Medical Sciences, Sehore (M.P.)

Scheme of Examination

First Semester –M.Tech. (VLSI Design)

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End Sem. Exam.	Tests (Two)	Assignments/ Quiz	End Sem. Practical / Viva	Practical Record/ assignment/Quiz/Presentation	
1.	MEVD-101	Advanced Mathematics	3	1	-	4	70	20	10	-	-	100
2.	MEVD-102	VLSI Design Concepts	3	1	-	4	70	20	10	-	-	100
3.	MEVD-103	Modeling of Digital Systems using HDL	3	1	-	4	70	20	10	-	-	100
4.	MEVD-104	Advanced Digital Signal Processing	3	1	-	4	70	20	10	-	-	100
5.	MEVD-105	VLSI Technology	3	1	-	4	70	20	10	-	-	100
6.	MEVD-106	Lab -1 : VLSI Design	-	-	6	6	-	-	-	90	60	150
7.	MEVD-107	Lab -2 : Hardware Description Languages	-	-	6	6	-	-	-	90	60	150
		Total	15	5	12	32	350	100	50	180	120	800

L: Lecture- T: Tutorial- P: Practical

w.e.f. July- 2014