Sri Satya Sai University of Technology & Medical Sciences, Sehore (M.P)

Scheme of Examination - CBCS Pattern(For B.E-2016 Batch)

Academic Year 2017– 2018

Branch : Electronics and Communications Engineering **Semester - IV**

S.No.	Subject Code	Subject Name	Maximum Marks Theory Slot			Maximum Marks (Practical Slot)		Periods/ hour/ week			Credits	Total Marks
			End Sem. Exam.	Mid Tests	Assign-ments/Quiz	End Sem. Practical & Viva	Practical Record /Assignment/ Quiz / Presentation	L	T	P		
1	ECC - 401	Linear Integrated Circuits	60	30	10	30	20	2	1	2	4	150
2	ECC - 402	Microprocessors and Microcontrollers	60	30	10	30	20	2	1	2	4	150
3	ECC - 403	Communication Networks and Transmission Lines	60	30	10	30	20	2	1	2	4	150
4	ECC - 404	Analog Communication	60	30	10	30	20	2	1	2	4	150
5	ECC - 405	Electromagnetic Theory	60	30	10	_	_	2	1	_	3	100
6	ECC - 406	Data Structure	60	30	10	30	20	2	1	2	4	150
TOTAL			**360**	**180**	**60**	**150**	**100**	**12**	**6**	**10**	**23**	**850**