School of Engineering

Sri Satya Sai University of Technology and Medical Sciences, Sehore

Curriculum for

Postgraduate Degree Courses in Engineering & Technology

Master of Technology (Electronics and Communication Engineering)

Specialization: VLSI

1) **Vision :** To achieve academic excellence in Electronics Engineering for advance masters by imparting in depth knowledge to the students, facilitating research activities and cater to the ever changing industrial demands, global and societal needs.

2) Mission :

1. To impart quality engineering education in DIGITAL COMMUNICATION & VLSI Field.
2. To provide technical expertise along with professional ethics as per societal needs.
3. To provide a creative environment through structured teaching - learning process.
4. To achieve academic excellence.
5. To strive towards efficient industry-institute interaction.
6. To serve the needs of the society through R&D activities.
7. To inculcate self learning attitude , entrepreneurial skills and professional ethics.

3)Program Educational Objectives (PEO's)

PEO-1 The post-graduates of VLSI Design will demonstrate their outstanding education skills that will enable them to integrate undergraduate fundamentals with the knowledge acquired to evaluate and analyse new developments in VLSI industry.
PEO-2 The post-graduates of VLSI Design will demonstrate advancement in engineering to engage in perpetual learning in order to suit multidisciplinary situations.
PEO-3 The post-graduates of VLSI Design would undertake a significant research or development projects.

4)Program Outcomes (PO's):

PO-1 Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialisation to the solution of complex engineering problems.

PO-2 Problem analysis: Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.

PO-3 Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specific needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO-4 Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO-5 Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO-6 The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO-7 Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO-8 Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO-9 Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO-10 Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO-11 Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO-12 Life-long learning: Recognise the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

5)Programme Specific Outcomes (PSO's):

PSO-1 Solve problems asked in competitive examinations of repute such as GATE and IES.

PSO-2 Design algorithms and systems for applications in communications, signal processing, embedded system, electromagnetics and VLSI by using software tools such as MATLAB and Xilinx and hardware platforms such as Arduino, Spartan and Raspberry Pi.

PSO-3 Prepare technical reports and presentations using international document preparation software tools such as LATEX.

6) PEO/PO Mapping

PEO	PROGRAMME OUTCOMES											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
I	√	√	√	√	√	√	√	√	√	√	√	√
II			√	√			√			√	√	
III				√	√	√			√			
IV					√		√		√		√	√
V				√						√	√	√

7)Programme PO's and PSO's Mapping

S.NO	Semester	Name of the Courses/ POs(Basic, Core Electives, Projects, Internships etc.)	PO 1 Engineering Knowledge	PO 2 Problem Analysis	PO3 Design/ Development of Solution	PO4 Investigation	PO 5 Modern Tool Usage	PO 6 The Engineer and Society	PO7 Environment and Sustainability	PO 8 Ethics	PO9 Individual and Team Work	PO10 Communication	PO11 Project Management	PO 12 Life-Long Learning	PSO 1	PSO 2
1	Semester -Ist	Advanced Mathematics	*	*	*	*								*		
		VLSI Design Concepts	*	*		*								*		
		Modeling of Digital Systems using HDL	*	*	*	*	*			*		*		*		
		Advanced Digital Signal Processing	*	*	*	*	*								*	
		VLSI Technology	*	*	*				*						*	
		Lab - 1 : VLSI Design	*	*	*	*	*			*	*	*		*	*	*
		Lab - 2 : Hardware	*	*	*	*	*			*	*		*	*		

		Description Languages													
2	Semester - IInd	Design of Analog/Mixed Mode VLSI Circuits	*	*	*	*								*	*	
		ASIC Design And FPGAs	*	*	*	*			*	*					*	
		Embedded Real Time Operating Systems	*	*	*	*			*					*	*	
		Embedded Systems	*	*	*	*										*
		System on Chip	*	*	*	*	*		*	*			*			
		Lab - 1 : Designing with FPGAs	*	*	*	*	*								*	
		Lab - 2 : Digital Signal Processing And Embedded	*	*	*	*	*								*	*

		System														
3	Semester - IIIrd	(a)CAD for VLSI Circuits	*	*	*	*	*								*	*
		(B) Design for Testability	*	*	*	*	*								*	*
		(A) VLSI SIGNAL PROCESSING	*	*	*	*	*		*							
		(B) Low Power and High Speed VLSI	*	*	*	*	*								*	*
		Seminar			*		*	*	*	*		*	*	*		
		Dissertation Part I	*	*	*	*			*		*					
4	Semester-IV	Dissertation Part- II	*	*	*	*	*	*	*		*			*	*	*

8)<u>Structure of Program.</u>

To fulfill the need of development of all the POs/ GAs, as per above mapping, the following semester wise program structure are as under.

<u>[L= Lecture, T = Tutorials, P = Practical's & C = Credits]</u>

Total Credits*= 104

Structure of Post Graduate Engineering program:

S. No.	Course Category	Credits of the VLSI Curriculum
1.	Program Core Corse	64
2.	Program Elective Course	08
4.	Project	32
5.	Audit Course	Nil
	Total	**104**

9)Scheme of Exanimation (VLSI) Academic Year 2019-20

Scheme of Examination

First Semester –Master of Technology (VLSI)

SEMESTER-I

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End Sem. Exam.	Tests (Two)	Assignments/ Quiz	End Sem. Practical / Viva	Practical Record/ assignment/Quiz/Presentation	
1.	MEVD-101	Advanced Mathematics	3	1	-	4	70	20	10	-	-	100
2.	MEVD-102	VLSI Design Concepts	3	1	-	4	70	20	10	-	-	100
3.	MEVD-103	Modeling of Digital Systems using HDL	3	1	-	4	70	20	10	-	-	100
4.	MEVD-104	Advanced Digital Signal Processing	3	1	-	4	70	20	10	-	-	100
5.	MEVD-105	VLSI Technology	3	1	-	4	70	20	10	-	-	100
6.	MEVD-106	Lab -1 : VLSI Design	-	-	6	6	-	-	-	90	60	150
7.7	MEVD-107	Lab -2 : Hardware Description Languages	-	-	6	6	-	-	-	90	60	150
		Total	15	5	12	32	350	100	50	180	120	800

Scheme of Examination

Second Semester –Master of Technology (VLSI)

SEMESTER-II

S.No.	Subject Code	Subject Name	Periods /week			Total Credits	Maximum Marks Allotted					Total Marks
							Theory Slot			Practical Slot		
			L	T	P		End Sem. Exam.	Tests (Two)	Assignments/ Quiz	End Sem. Practical / Viva	Practical Record/ assignment/ Quiz/ Presentation	
1.	MEVD-201	Design of Analog/Mixed Mode VLSI Circuits	3	1	-	4	70	20	10	-	-	100
2.	MEVD-202	ASIC Design And FPGAs	3	1	-	4	70	20	10	-	-	100
3.	MEVD-203	Embedded Real Time Operating Systems	3	1	-	4	70	20	10	-	-	100
4.	MEVD-204	Embedded Systems	3	1	-	4	70	20	10	-	-	100
5.	MEVD-205	System on Chip	3	1	-	4	70	20	10	-	-	100
6.	MEVD-206	Lab -1 : Designing with FPGAs	-	-	6	6	-	-	-	90	60	150
7.	MEVD-207	Lab -2 : Digital Signal Processing And Embedded System	-	-	6	6	-	-	-	90	60	150
		Total	15	5	12	32	350	100	50	180	120	800

Scheme of Examination

Third-Semester –Master of Technology (VLSI)

SEMESTER-III

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End Sem. Exam.	Tests (Two)	Assignments/ Quiz	End Sem. Practical / Viva	Practical Record/ assignment/Quiz/Presentation	
1.	MEVD-301	Elective- I	3	1	-	4	70	20	10	-	-	100
2.	MEVD-302	Elective- II	3	1	-	4	70	20	10	-	-	100
3.	MEVD-303	Seminar			4	4				-	100	100
4.	MEVD-304	Dissertation Part I			8	8				120	80	200
		Total	6	2	12	20	140	40	20	120	180	500

Elective -1	(A) CAD for VLSI Circuits	(B) Design for Testability
Elective - 2	(A) VLSI SIGNAL PROCESSING	(B) Low Power and High Speed VLSI Design

Scheme of Examination

Fourth- Semester –Master of Technology (VLSI)

SEMESTER-IV

S.No.	Sub Code	Subject Name	Periods per			Credits	Max Marks Theory			Max. Marks Practical		Total Marks
			L	T	P		End Sem Exam	Mid Sem	TW	End Sem Practical / Viva	Practical Record/Quiz /Assignment / Presentation	
1.	MEVD-401	Dissertation Part- II	-		20	20	-	-	-	300	200	500
TOTAL			-		20	20	-	-	-	300	200	500

Advanced Mathematics

MEVD- 101

MEVD-101	Advanced Mathematics	3L:1T:0P	4 credits	4Hrs/Week

Course Preamble:

1. To learn principles of advanced engineering mathematics through linear algebra and calculus of variations.
2. To understand probability theory and random process that serve as an essential tool for applications of electronics and communication engineering sciences.

Course Outcomes:

1. Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
2. Apply the technique of singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.
3. Utilize the concepts of functional and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.

UNIT 1: (10-HOURS)

Partial Differential Equation Solution of Partial Differential Equation (PDE) by separation of variable method, Numerical solution of PDE (Laplace, Poisson's, Parabola) using finite difference Methods.

UNIT 1I: (10-HOURS)

Matrices And Linear System Of Equations Solution of linear simultaneous equations by Gaussian elimination and its modification, Crout's triangularization method, Iterative methods-Jacobins method, Gauss-Seidal method, Determination of Eigen values by iteration.

UNIT 1II: (10-HOURS)

Calculus Of Variations Euler-Lagrange's differential equation, The Brachistochrone problems and other applications. Isoperimetric problem, Hamilton's Principle and Lagrange's Equation, Rayleigh-Ritz method, Galerkin method.

UNIT 1V: (06-HOURS)

Fuzzy Logic Operations of fuzzy sets, fuzzy arithmetic & relations, fuzzy relation equations, fuzzy logics. MATLAB introduction, programming in MATLAB scripts, functions and their application.

UNIT V: (06-HOURS)

Reliability Introduction and definition of reliability, derivation of reliability functions, Failure rate, Hazard rate, mean time t future & their relations, concepts of fault tolerant analysis.

Reference Books:

1. Higher Engineering Mathematics - by Dr. B.S. Grewal; Khanna Publishers

2. Calculus of Variations - by Elsgole; Addison Wesley.

3. Applied Numerical Methods with MATLAB by Steven C Chapra, TMH.

4. Introductory Methods of Numerical Analysis by S.S. Shastry,

5. Calculus of Variations - by Galfand & Fomin; Prentice Hall.

6. Higher Engineering Mathematics by B.V. Ramana, Tata Mc Hill.

7. Advance Engineering Mathematics by Ervin Kreszig, Wiley Easten Edd.

8. Numerical Solution of Differential Equation by M. K. Jain

9. Numerical Mathematical Analysis By James B. Scarborogh

10. Fuzzy Logic in Engineering by T. J. Ross

11. Fuzzy Sets Theory & its Applications by H. J. Zimmersoms

VLSI Design Concepts

MEVD-102

MEVD-102	VLSI Design Concepts	3L:1T:0P	4 credits	4Hrs/Week

Course Preamble:

1. To design and optimize CMOS Digital Integrated Circuits.
2. To understand floor planning and layout issues for digital circuits

Course Outcomes:

1. Understand the basic Physics and Modelling of MOSFETs.
2. Learn the basics of Fabrication and Layout of CMOS Integrated Circuits.
3. Study and analyze the performance of CMOS Inverter circuits on the basis of their operation and working.
4. Study the Static CMOS Logic Elements

UNIT – I : Introduction to CMOS circuits: (10HOURS)

MOS transistors, MOS switches, CMOS logic: Inverter, combinational logic, NAND, NOR gates, compound gates, Multiplexers. Memory: Latches and registers. Circuit and system representations: Behavioral, structural and physical representations.

UNIT– II: MOS transistor theory: (10HOURS)

NMOS, PMOS enhancement mode transistors, Threshold voltage, body effect, MOS device design equations, MOS models, small signal AC characteristics, CMOS inverter DC characteristics, static load MOS inverters, Bipolar devices - advanced MOS modeling – large signal and small signal modeling for BJT.

UNIT– III: LOW – VOLTAGE LOW POWER VLSI CMOS CIRCUIT DESIGN: (10 HOURS)

CMOS invertor – Characteristics – Power dissipation. Capacitance estimation. CMOS static logic design, Logic styles.

UNIT– IV (10 HOURS)

Circuit characterization and performance estimation: Estimation of resistance, capacitance, inductance. Switching characteristics, CMOS gate transistor sizing, power dissipation, sizing routing conductors, charge sharing, Design margining yield, reliability. Scaling of MOS transistor dimensions.

UNIT– V (10 HOURS)

CMOS circuit and logic design: CMOS logic gate design, physical design of simple logic gates. CMOS logic structures. Clocking strategies, I/O Structures.

REFERENCES

1. Weste, Eshraghian, “Principles of CMOS VLSI design”, 2nd Edition Addison Wesley, 1994.

2. Douglas A Pucknell and Kamaran Eshragian, “ Basic VLSI design “, 3rd edition, PHI, 1994.

3. BELLAOUR & M.I.ELAMSTRY, “Low – Power Digital VLSI Design, Circuits and Systems”, Kluwer Academic Publishers, 1996.

4. S.IMAM & M.PEDRAM, “Logic synthesis for Low – Power VLSI Designs”, Kluwer Academic publishers, 1998.

5. B.G.K.YEAP, “Practical Low Power Digital VLSI Design”, Kluwer Academic publishers, 1998.

Modeling of Digital Systems using HDL

MEVD-103

MEVD-103	Modeling of Digital Systems using HDL	3L:1T:0P	4 credits	4Hrs/Week

Course Preamble:

1. To design combinational, sequential circuits using Verilog HDL.
2. To understand behavioral and RTL modeling of digital circuits
3. To verify that a design meets its timing constraints, both manually and through the use of computer aided design tool.

Course Outcomes:

1. Understand the basic concepts of verilog HDL
2. Model digital systems in verilog HDL at different levels of abstraction
3. Know the simulation techniques and test bench creation.

UNIT – I Introduction to PLDs & FPGAs (10 HOURS)

ROMs, Logic array (PLA), Programmable array logic, GAL, bipolar PLA, NMOS PLA, PAL 14L4, Xilinx logic cell array (LCA) – I/O Block – Programmable interconnect – Xilinx – 3000 series and 4000 series FPGAs. Altera CPLDs, altera FLEX 10K series PLDs.

UNIT – II Placement and routing (10 HOURS)

Mincut based placement – iterative improvement placement– Routing: Segmented channel routing – Maze routing – Routability and routing resources – Net delays.

UNIT – III Introduction to VHDL (10 HOURS)

Digital system design process – Hardware simulation – Levels of abstraction – VHDL requirements – Elements of VHDL – Top down design VHDL operators – Timing – Concurrency – Objects and classes – Signal assignments – Concurrent and sequential assignments.

UNIT – IV (6 HOURS)

Structural, Data flow & Behavioral description of hardware in VHDL Parts library – Wiring of primitives – Wiring of iterative networks – Modeling a test bench – Top down wiring components – Subprograms. Multiplexing and data selection – State machine descriptions – Open collector gates – Three state bussing. - Process statement – Assertion statement – Sequential wait statements – Formatted ASCII I/O operations MSI based design.

UNIT – V (10HOURS)

Introduction to Verilog HDL Lexical conventions – Data types – System tasks and Compiler Directives- Modules and Ports- Gate Level Modeling with Examples.

REFERENCES

1. P.K. Chan & S. Mourad, "Digital Design sing Field Programmable Gate Array" 1st Edition, Prentice Hall,

1994.

2. J. V. Old Field & R.C. Dorf, " Field Programmable Gate Array", John Wiley, 1995.

3. M. Bolton, " Digital System Design with Programmable Logic", Addison Wesley, 1990.

4. Thomas E. Dillinger, " VLSI Engineering", Prentice Hall, 1st Edition, 1998.

5. Douglas Perry, "VHDL", 3rd Edition, McGraw Hill 2001.

6. J. Bhasker, "VHDL", 3rd Edition, Addison Wesley, 1999

Advanced Digital Signal Processing

MEVD-104

MEVD-104	Advanced Digital Signal Processing	3L:1T:0P	4 credits	4Hrs/Week

Course Preamble:

1. To Comprehend characteristics of discrete time signals and systems
2. To analyze and process signals using various transform techniques
3. To identify various factors involved in design of digital filter

Course Outcomes:

1. Analyze and process signals in the discrete domain
2. Design filters to suit specific requirements for specific applications
3. Perform statistical analysis and inferences on various types of signals

UNIT 1 : (10 HOURS)

Discrete Time signals - sequences, representation Discrete Time Systems Linear, Time invariant, LTI System, properties, constant coefficient difference equation. Frequency Domain Representation of discrete time signals & systems

UNIT 2 : (10 HOURS)

Discrete Time Random Signals Z Transform properties, R.O.C, stability, Causality criterion,Inverse Z-Transform , Recursive and Non recursive systems, Realization of discrete time system.

UNIT 3 : (10 HOURS)

D.F.T â□“ properties, linear and circular convolution Discrete Cosine transform, relationship between DFT & DCT, I.D.F.T , computation of D.F.T : F.F.T â□“ Decimation in time & Decimation in frequency.

UNIT -4 (6 HOURS)

F.I.R and I.I.R Systems : Basic structure of FIR & IIR, Bilinear transformation, Design of discrete time I.I.R filters â□“ Butterworth, Chebychev, Inv. Chebychev, elliptic etc. Design of F.I.R filters by windowing â□“ rectangular, Bartlett, Hann, Hamming, Kaiser window filter , Design method , Relationship of Kaiser to other windows. Application of MATLAB for design of digital filters Effect of finite register length in filter design.

UNIT 5 (6 HOURS)

Advanced signal processing techniques and transforms: Multirate Signal processing Down sampling/upsampling, Int. to discrete Hilbert transform, wavelet transform, Haar transform etc. Application of DSP to Speech Signal Processing.

REFERENCES :

1. A.V Opprenheim and R.W Schaffer, â□œDiscrete â□“ Time signal processingâ€• (2nd edition) , Prentice Hall

2. S. Mittra Digital Signal Processing using MATLAB, 2nd Edition.

3. Proakis, Int. to Digital Signal Processing, Maxwell Mcmillan.

VLSI Technologies

MEVD -105

MEVD-105	VLSI Technologies	3L:1T:0P	4 credits	4Hrs/Week

Course Preamble:

1. To design and optimize CMOS Digital Integrated Circuits.
2. To understand floor planning and layout issues for digital circuits

Course Outcomes:

1. Understand the need for low power in VLSI.
2. Understand various dissipation types in CMOS.
3. Estimate and analyse the power dissipation in VLSI circuits. Course Outcomes:

UNIT –I: (10 HOURS)

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II: (10 HOURS)

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III: (10 HOURS)

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV: (6 HOURS)

Sequential Systems: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V: (6 HOURS)

Floor Planning: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

REFERENCE:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.

2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.

4. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

MEVD-106

Lab -1 : VLSI Design

MEVD-106	VLSI Design	0L:0T:6P	6 credits	6Hrs/Week

EXPRIMENT LIST

1. Design a full adder circuit layout having a and b as input cin as Previous carry and Sum & Cout as output, according to design rules then verify results by simulating the design.
2. Design CMOS layout for D Flip-flop according to design rules then verify results by simulating the design.
3. Design a 4X1 Multiplexer using 2X1 Multiplexer then design a CMOS layout for it according to design rules then verify results by simulating the design.
4. Design a D Latch using pass gates and inverters then design a CMOS layout for it according to design rules then verify results by simulating the design.
5. Design a 2X1 Multiplexer using pass gates then design a CMOS layout for it according to design rules then verify results by simulating the design.
6. Design CMOS layout for an 2 input NAND Gate according to design rules then verify results by simulating the design**.**

MEVD-107

Lab -2 : Hardware Description Languages

MEVD-107	Lab -2 : Hardware Description Languages	0L:0T:6 P	6 credits	6Hrs/Week

EXPRIMENT LIST

1. Write Verilog code to realize all the gates.
2. Write a Verilog program for the following combinational designsa).
(A) 2 to 4 decoder b).
(B) 8 to 3 (encoder without priority & with priority)c).
(C) 8 to 1 multiplexerd). 4 bit binary to gray convertere).
(D) Multiplexer,
(E) de-multiplexer,
(F) comparator.

3. Write a HDL code to describe the functions of a full adder using three modeling styles.
4 .Write a model for 32 bit ALU using the schematic diagram shown below A(31:0)

5. Develop the Verilog code for the following flip-flops SR, D, JK &
6. Design 4 bit binary, BCD counters (Synchronous reset and asynchronous reset) and "anysequence counters Using Verilog code

MEVD-201 CMOS Mixed Signal Circuit Design

MEVD-201	CMOS Mixed Signal Circuit Design	3L:1T:0P	4 credits	4Hrs/Week

Course Preamble:

1. To design and optimize CMOS Mixed Signal Circuit Design.
2. To understand floor planning and layout issues for digital circuits

Course Outcomes:

1. To learn performance optimization techniques in VLSI signal processing,
2. Transformations for high speed and power reduction using pipelining, retiming, parallel processing techniques, supply voltage reduction as well as for strength or capacitance reduction,
3. Area reduction using folding techniques, Strategies for arithmetic implementation,

UNIT -I: Switched Capacitor Circuits: (10 HOURS)
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT -II: Phased Lock Loop (PLL): (10 HOURS)
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT -III: Data Converter Fundamentals: (10 HOURS)
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV: Nyquist Rate A/D Converters: (6 HOURS)
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D
converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V: Oversampling Converters: (6 HOURS)

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

Reference Books:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press,
International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013
4. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
5. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
6. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

MEVD -202
ASIC Design and FPGA

MEVD-202	ASIC Design and FPGA	3L:1T:0P	4 credits	4Hrs/Week

Course Preamble:

1. To design and optimize ASIC Design and FPGA.
2. To understand floor planning and layout issues for digital circuits

Course Outcomes:

1. Model digital systems in VHDL and SystemC at different levels of abstraction.
2. Partition a digital system into different subsystems.
3. Simulate and verify a design.

UNIT -I: Introduction To ASICS (10 HOURS)
Introduction to ASICS, CMOS Logic And ASIC Library Design, Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort - Library cell design - Library architecture.

Unit -II: Programmable Asics (10 HOURS)
Programmable Asics, Programmable ASIC Logic Cells And Programmable ASIC I/O Cells, Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA - Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

Unit -III: Interconnect (10 HOURS)
Programmable ASIC Interconnect, Programmable ASIC Design Software And Low Level Design Entry Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000,- Altera FLEX - Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools - EDIF- CFI design representation.

Unit -IV: Construction (6 HOURS)

ASIC Construction, Floor Planning, Placement And Routing, System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow - global routing - detailed routing - special routing - circuit extraction - DRC.

UNIT -V: PLDs (6 HOURS)

Design using Xilinx family FPGA, Review of VHDL/Verilog: Entities and architectures.

Reference Books:

1. M.J.S .Smith, - " Application - Specific Integrated Circuits " - Addison -Wesley Longman Inc., 1997
2. Skahill, Kevin," VHDL for Programmable Logic", Addison-Wesley, 1996
3. John F. Wakherly, " Digital Design: Principles and Practices", 2nd Edn 1994, Prentice Hall International Edn
4. Charles W. Mckay, "Digital Circuits a proportion for microprocessors", Prentice Hall

Embedded Real Time Operating Systems

MEVD-203	Embedded Real Time Operating Systems	3L:1T:0P	4 credits	4Hrs/Week

Course Preamble:

1. Introduction of the real-time systems.
2. Computing required for the real-time embedded systems.
3. Communication required for the real-time embedded systems

Course Outcomes:

1. To present the mathematical model of the system.
2. To develop real-time algorithm for task scheduling.
3. To understand the working of real-time operating systems and real-time database.
4. To work on design and development of protocols related to real-time communication

UNIT – I: Introduction (10 HOURS)

Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec.

UNIT - II: Real Time Operating Systems (10 HOURS)

Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III: Objects, Services and I/O (10 HOURS)

Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV: Exceptions, Interrupts and Timers (6 HOURS)

Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V: Case Studies of RTOS (6 HOURS)

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

Reference Books:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011
2. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
3. Advanced UNIX Programming, Richard Stevens
4. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

Embedded System Design

MEVD-204	Embedded System Design	3L:1T:0P	4 credits	4Hrs/Week

Course Preamble:

1. To provide an overview of Design Principles of Embedded System.
2. To provide clear understanding about the role of firmware , operating systems in correlation with hardware systems.

Course Outcomes:

1. Expected to understand the selection procedure of Processors in the Embedded domain.
2. Design Procedure for Embedded Firmware.
3. Expected to visualize the role of Real time Operating Systems in Embedded Systems

UNIT - I: Embedded Processing: (10 HOURS)

Introduction to Embedded Computing, Difference between Embedded and General-Purpose Computing, Characterizing Embedded Computing, Design Philosophies, RISC, CISC, VLIW versus superscalar, VLIW versus DSP Processors, Role of the Compiler, Architectural structures, The datapath, Registers and Clusters, Memory Architecture, Branch architecture, Speculation and prediction, Prediction in the embedded domain, Register File Design, Pipeline Design, the control unit, control registers.

UNIT - II: Embedded Processors: (10 HOURS)

Microprocessor versus Microcontroller architecture, ARM architecture, Embedded Cores, Soft and Hard Cores, Architecture of Configurable Microblaze soft core, Instruction set, Stacks and Subroutines, Microblaze Assembly Programming, Input-Output interfacing, GPIO, LCD interfacing, Peripherals, DDR Memory, SDRAM, Microblaze interrupts, Timers, Exceptions, Bus Interfacing, DMA, On-chip Peripheral bus (OPB), OPB Arbitration, OPB DMA.

UNIT -III: RTOS and Application design (10 HOURS)

Programming language choices, Traditional C and ANSI C, C++ and Embedded C++, matlab, Embedded JAVA, Embedded C extensions, Real time operating systems, Embedded RTOS, Real time process scheduling, structure of real time operating system, Memory management in Embedded operating system, operating system overhead, interprocess communication mechanisms, File systems in Embedded devices, Different types of locks, Semaphores, Application studies with Vxworks, Montavista Linux etc.

UNIT -IV System Design and Simulation: (6 HOURS)

System-on-a-Chip (SoC), IP Blocks and Design Reuse, Processor Cores and SoC, Non-programmable accelerators, reconfigurable logic, multiprocessing on a chip, symmetric multiprocessing, heterogeneous multiprocessing, use of simulators, Compilers, Loaders, Linkers, locators, assemblers, Libraries, post run optimizer, debuggers, profiling techniques, binary utilities, linker script, system simulation, In Circuit Emulation, Validation and verification, Hardware Software partitioning, Co-design.

UNIT - V: Laboratory Work (6 HOURS)

Embedded System design using Embedded Development Kit Software and implementation on FPGA hardware, Practicals on Xilkernel, Vxworks and montavista Linux Real Time Operating Platforms.

Reference Books::

1. Wolf, W., High-Performance Embedded Computing Architectures, Applications,
2. and Methodologies, Morgan Kaufman Publishers (2007).
3. Heath, S., Embedded Systems Design, Elsevier Science (2003).
4. Fisher, J.A., Faraboschi, P. and Young, C., Embedded Computing - A VLIW
5. Approach to Architecture, Compilers and Tools, Morgan Kaufman (2005).
6. Simon, D.E., An Embedded Software Primer, Dorling Kindersley (2005).

MEVD-205
System on Chip

MEVD-205	System on Chip	3L:1T:0P	4 credits	4Hrs/Week

Course Preamble:

1) To introduce the architectural features of system on chip.
2) To provides information on interconnection necessities between computational block and memory block.

Course outcomes:

1) Introduction to SOC Architecture and design.
2) Processor design Architectures and limitations
3) To acquires the knowledge of memory architectures on SOC.
4) To understands the interconnection strategies and their customization on SOC.

Unit I – Introduction (10 HOURS)

Introduction to SoC Design., Platform-Based SoC Design., Multiprocessor SoC and Network on Chip, Low-Power SoC Design

Unit II - System Design With Model Of Computation And Co-Design (10 HOURS)

System Models, Validation and Verification, Hardware/Software Codesign Application Analysis, Synthesis.

Unit III - Computation–Communication Partitioning And Network On Chip-Based Soc (10 HOURS)

Communication System: Current Trend, Separation of Communication and Computation. Communication-Centric SoC Design, Communication Synthesis, Network-Based Design, Network on Chip, Architecture of NoC

Unit IV - Noc Design

Practical Design of NoC, NoC Topology-Analysis Methodology, Energy Exploration, NoC Protocol Design, Low-Power Design for NoC: Low-Power Signaling, On-Chip Serialization, Low-Power Clocking, Low-Power Channel Coding, Low-Power Switch, Low-Power Network on Chip Protocol

Unit V - Noc /Soc Case Studies

Real Chip Implementation-BONE Series-,BONE 1-4, Industrial Implementations-,Intel's Tera-FLOP 80-Core NoC, Intel's Scalable 31,Communication Architecture, Academic Implementations-FAUST, RAW; design case study of SoC –digital camera

Reference Books:

1. Hoi-jun yoo, Kangmin Lee, Jun Kyoung kim, "Low power NoC for high performance SoC desing",CRC press, 2008.
2. Vijay K. Madisetti Chonlameth Arpikanondt, "A Platform-Centric Approach to System-on-Chip (SOC) Design", Springer, 2005

MEVD-206
Lab -1 : Designing with FPGAs

MEVD-206	Lab -1 : Designing with FPGAs	0L:0T:6P	6 credits	6Hrs/Week

EXPERIMENT LIST

1 .XILINX's VIVADO FPGA Tools

2 . Simple Combinational Logic

3. Multi-Function Gate

4. Three-Bit Binary Added

5. Multiplexers in Combinational logic design

6. Decoder and Demultiplexer

7. Random Access Memory

8. Flip-Flop Fundamentals

9. Designing with D-Flip flops: Shift Register and Sequence Counter

10 Sequential Circuit Design: Counter with Inputs

MEVD-207

Lab -2 : Digital Signal Processing And Embedded System

MEVD-207	**Lab -2 : Digital Signal Processing And Embedded System**	**0L:0T:6P**	**6 credits**	**6Hrs/Week**

EXPERIMENT LIST

1. Study of MATLAB 7.0
2. Arithmatic operation using MATLAB 7.0
3. Generation of Signals
4. Linear convolution using MATLAB
5. Program illustrates the design of a Butterworth bandstop filter.
6. To implement a causal IIR filter implemented in the Direct Form II structure, the function direct2 given below can be employed.
7. To implement a causal IIR filter implemented in the Direct Form II structure, the function direct2 given below can be employed
8. Program illustrates the design of a causal IIR filter, its simulation in transposed Direct Form II, and its application in filtering a signal.
9. Program up-sampler.
10. Illustration of Down-Sampling by an Integer Factor
11. Use fir2 to create a bandlimited input sequence
12. Program P10 4 can be employed to study the frequency-domain properties of the downsampler
13. FIR filter using Rectangular Window
14. FIR filter using Hamming Window
15. Circular Convolution of two sequences using MATLAB
16. IIR filter design using MATLAB
17. Develop an embedded system for traffic light controller using microcontroller.
18. Develop an embedded system for automatic motion of a car & susequet display on LCD using microcontroller.

Elective-I
MEVD 301 (A) CAD for VLSI Circuits

MEVD-301	**(A) CAD for**	**3L:1T:0P**	**4 credits**	**4Hrs/Week**

	VLSI Circuits			

Course Preamble:

1. To design and optimize CAD for VLSI circuits.
2. To understand floor planning and layout issues for digital circuits

Course Outcomes:

1. Understand of VLSI Design Automation.
2. Acquire knowledge about CAD tools used for VLSI design.
3. Able to understanding Algorithms for VLSI Design Automation.
4. Able to gather knowledge of High Level Synthesis.
5. Understand Timing Analysis

UNIT- I VLSI DESIGN METHODOLOGIES : (10 HOURS)

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT -II DESIGN RULES (10 HOURS)

Layout Compaction - Design rules - problem formulation - algorithms for Iconstraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT- III FLOOR PLANNING : (10 HOURS)

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing – channel routing - global routing - algorithms for global routing.

UNIT -IV SIMULATION : (6 HOURS)

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V MODELLING AND SYNTHESIS : (6 HOURS)

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

REFERENCES

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002

MEVD 301 (B) Design for Testability

MEVD-301(B)	(B) Design for Testability	3L:1T:0P	4 credits	4Hrs/Week

Course Preamble:

1. To expose the students, the basics of testing techniques for VLSI circuits and Test Economics.

Course Outcomes:

1. Apply the concepts in testing which can help them design a better yield in IC design.
2. Tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.
3. Analyse the various test generation methods for static & dynamic CMOS circuits.
4. Identify the design for testability methods for combinational & sequential CMOS circuits.
5. Recognize the BIST techniques for improving testability.

UNIT -I: INTRODUCTION TO TESTING: (10 HOURS)

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II: Logic and Fault Simulation: (10 HOURS)

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -III: Testability Measures: (10 HOURS)

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV: BUILT-IN SELF-TEST:(6 HOURS)

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-PerScan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V: Boundary Scan Standard:

Motivation, System Configuration with Boundary Scan: TAP

Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan
Description Language: BDSL Description Components, Pin Descriptions.

REFERENCE

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Publishers.
2. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
3. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

Elective-II

MEVD 302 (A) VLSI SIGNAL PROCESSING

MEVD-302(A)	**VLSI SIGNAL PROCESSING**	**3L:1T:0P**	**4 credits**	**4Hrs/Week**

Couse Preamble:

1. Introduce students to the fundamentals of VLSI signal processing and expose them to examples of applications.
2. Design and optimize VLSI architectures for basic DSP algorithms.
3. Design and optimize VLSI architectures for basic DSP algorithms.

Course Outcomes:

1. Understand VLSI design methodology for signal processing systems.
2. Be familiar with VLSI algorithms and architectures for DSP.
3. Be able to implement basic architectures for DSP using CAD tools.

UNIT -I: INTRODUCTION TO DSP: (10 HOURS)

Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT –II: FOLDING AND UNFOLDING: (10 HOURS)

Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT -III: SYSTOLIC ARCHITECTURE DESIGN: (10 HOURS)

Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT -IV: FAST CONVOLUTION: (6 HOURS)

Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT -V: LOW POWER DESIGN: (6 HOURS)

Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

REFERENCE

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.
3. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice Hall.
4. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

MEVD 302 (B) Low Power VLSI Design

MEVD-302(B)	**Low Power VLSI Design**	**3L:1T:0P**	**4 credits**	**4Hrs/Week**

Course Preamble:

1. This course addresses a profound analysis on the development of the CMOS & BiCMOS digital circuits for a low voltage low power environment.
2. To study the concepts of device behavior and modelling.
3. To study the concepts of low voltage, low power logic circuits.

Course Outcomes:

RSE OUTCOME:-

1. Capability to recognize advanced issues in VLSI systems, specific to the deepsubmicron silicon technologies.
2. Students able to understand deep submicron CMOS technology and digital CMOS design styles.
3. To design chips used for battery-powered systems and high performance circuits.

UNIT –I: FUNDAMENTALS: (10 HOURS)

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II: LOW-POWER DESIGN APPROACHES: (10 HOURS)

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III: LOW-VOLTAGE LOW-POWER ADDERS: (10 HOURS)

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low Voltage Low-Power Logic Styles.

UNIT –IV: LOW-VOLTAGE LOW-POWER MULTIPLIERS: (6 HOURS)

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V: LOW-VOLTAGE LOW-POWER MEMORIES: (6 HOURS)

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

REFERENCE :

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
4. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
5. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
6. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
7. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
8. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, Anatha Chandrakasan, Springer, 2005.

MEVD-303
Seminar

MEVD-303	**Seminar**	**0L:0T:4P**	**4 credits**	**4Hrs/Week**

Course Preamble : To Analyses the topic of seminar with scope of work.

Course Outcome: This course helps to collect useful information from the literature on the assigned topic.

Seminar topic: One faculty assigned to each M. Tech student. Usually the assigned faculty suggest a particular research topic to the concern student. Subsequently student collects research papers. The faculty assigned/ supervisor gives one / two research paper and advice the student to make detail study on a. Authors contribution b. Mathematical analysis c. Performance comparison parameters

MEVD-304
Dissertation Part I

MEVD-304	**Dissertation Part I**	**0L:0T:8P**	**8 credits**	**6Hrs/Week**

Course Preambles: To analyze the title and proposed a model for Dissertation.

Course outcomes: To study of literature survey, formulate the research problem and develop necessary methodology related to research problem. A workable design/ algorithm to be developed based on the proposed methodology, algorithm a design to be noted.

Course Contents: Title of the Dissertation- This should be carefully decided by the student after discussing with the dissertation supervisor or the guide. Explain the relevance and importance of the dissertation; Write a brief (1 or 2 pages) introduction of the dissertation explaining its relevance and importance.

Student has to spend two hours daily in library to analyze the problem. It is also essential for student to meet supervisor twice in a week to discuss the research problem. After four weeks of registration the first evaluation has been done before committee to revive the literature survey and formulation of the problem. .In second the evaluation, the student has to show the progress of work in terms of design level, mathematical model/ algorithm etc. At end of semester, simulation based design has been analyzed by the committee.

MEVD- 401
Dissertation Part- II

MEVD-401	**Dissertation Part**	**0L:0T:20P**	**20 credits**	**6Hrs/Week**

	II			

NOTES1.

Dissertation ** to be continued from III semester.
2. Final evaluation of dissertation will be based on the cumulative performance in all III and IV.
3. It is desirable to have one publication from the dissertation.